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Power Optimized Comparator Design Using Reversible TR and UPG

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ABSTRACT

The development of high-speed comparators is essential for numerous digital applications, particularly where quick decision-making is crucial, such as in real-time processing and high-speed arithmetic operations. Low delay in comparator circuits significantly enhances the overall system performance by reducing latency, which is the time taken for a signal to propagate through the circuit. A reversible binary tree comparator, structured with 2-bit reversible binary comparators, offers a promising solution. Each node in this binary tree comparator compares two 2-bit numbers and generates outputs indicating the comparison result. The proposed 2-bit comparator utilizes TR and UPG gates, achieving improved performance metrics such as reduced quantum cost and delay. The TR gate is particularly efficient, producing necessary logic functions without additional NOT gates, thereby optimizing the design. By modifying traditional logic equations, the design maps efficiently onto the TR gate's capabilities, further minimizing delay and enhancing speed. This work underscores the importance of designing low- latency, high-speed comparators to meet the demands of modern high-performance computing systems.

INTRODUCTION

A reversible logic gate is an n-input, n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs but also the inputs can be uniquely recovered from the outputs. Extra inputs or outputs are added so that the number of inputs is made equal to the number of outputs whenever it is necessary. An important constraint present on the design of a reversible logic circuit using reversible logic gate is that fan-out is not allowed. A reversible circuit should be designed using minimum number of reversible gates. The three major design goals of reversible logic are as follows. First, minimization of the quantum cost - the number of 1*1 and 2*2 reversible calculations necessary to generate the logical output - will reduce the device's computational complexity. Second, minimization of the delay - the logical depth of the device – will improve the throughput of the device. Third, reduction of the ancillary inputs and garbage outputs - inputs and outputs not implemented in the

design of the gate and only serve to maintain reversibility of the device – will improve the design space require to implement the logic.

LITERATURE SURVEY:

Traditional comparator designs, like CMOS-based comparators, focus on speed and power efficiency. However, they often suffer from significant energy dissipation and larger circuit sizes. Recent advancements have introduced reversible logic into comparator designs, which aim to reduce energy loss and circuit complexity. Works by Toffoli and Fredkin have laid the groundwork for reversible gates that are now being integrated into comparator circuits. Binary tree comparators are widely used in digital systems for efficient sorting and comparison operations. Conventional designs utilize irreversible logic gates, leading to energy inefficiency. Researchers have explored reversible binary tree structures to mitigate this issue. For instance, the work by Gupta et al. on reversible arithmetic operations provides a foundation for developing energy-efficient binary tree comparators. Evaluating the performance of reversible comparators involves metrics such as quantum cost and delay. Quantum cost refers to the number of basic quantum operations needed to implement a circuit, while delay measures the time required for signal propagation. Research by Mohammadi et al. provides a comprehensive analysis of these metrics, guiding the design of high-performance reversible comparators. The need for high-speed and energy-efficient comparators is evident in high-performance computing (HPC) applications. Reversible comparators play a crucial role in parallel processing, real- time data analysis, and high-speed arithmetic operations. The work by Shende et al. on the application of reversible logic in HPC systems underscores the importance of optimizing comparator designs for these environments.

EXISTING WORK

The proposed reversible binary tree comparator has a binary tree structure in which each node consists of a 2-bit reversible binary comparator that can compare two 2-bit numbers x(xi, xi−1) and y(yi, yi−1), to generate 2-bit outputs indicating whether x(xi, xi−1)>y(yi, yi−1) or x(xi, xi−1)y or xy) and O2(x=y).

For designing the 2-bit reversible binary comparator, consider two 2-bit binary numbers x(x1, x0) and y(y1, y0). The condition for x>y: (x1 > y1) or (x1 = y1 and x0 > y0). Thus Y = x1y^{-}1+kx0y^{-}0 should be 1 for x>y, where k = x1⊕y1 is 1 when x1 = y1. Similarly, the condition for x<y: (x1 < y1) or (x1 = y1 and x0 < y0). Thus Z = $^{-}$x1y1 + kx^{-}0y0 should be 1 for x<y, where k = x1⊕y1 is 1 when x1 = y1. From the above equations of Y and Z we observed that to design the 2-bit reversible binary comparator we need to have the reversible module that can generate the outputs as x1y^{-}1 andx^{-}1y1, the module is called R-B comp. Once we have R-B comp module ready it can also generate x0y^{-}0 and x^{-}0y0 by changing the inputs. We propose the reversible design of the R-B comp module using the reversible TR gate. TR gate is very useful as when its input C=0 we will have R = A · B^{-} which can implement the logic functions such as x1y^{-}1 and x^{-}1y1. Thus

we used TR gate to design the R-B comp module. In the R-B comp module the outputs $x^{-}1y1$ and $x1y^{-}1$ are labelled as a1 and b1, respectively. Further it can be observed that R-B comp also produces $^{-}k = x1 \oplus y1$ which is beneficial in the design of 2-bit comparator.

After careful analysis, we modified the logic equations of $Y = x1y^{-}1 + kx0y^{-}0$ and $Z = {}^{-}x1y1 + kx^{-}0y0$ to $Y = x1y^{-}1 \oplus kx0y^{-}0$ and $Z = {}^{-}x1y1 \oplus kx^{-}0y0$, respectively. This is because since any function F=A+BC will produce the same output as the function $F=A \oplus BC$ except when the variables A,B,C have the values as A=1,B=1 and C=1. In the equation of Y and Z explained above when k=1 then $x1y^{-}1$ and $x^{-}1y1$ will be 0 and vice versa, hence we are able to replace + operator with $\oplus$ operator without affecting the functionality of the design. This helps in mapping of the equations of Y and Z on the third output of the TR gate which is $R=AB^{-} \oplus C$. Since our R-B comp circuit shown in Fig. 5(a) produces the ^{-}k it can be passed as the B input of the TR gates to produce Y and Z signals without the need of the NOT gates. The R-B comp shown in Fig.5(a) along with CNOT gate and TR gate to design the 2-bit reversible comparator as shown in Fig.5(b). The 2-bit reversible comparator has 6 garbage outputs (the unused outputs in the design) and has the quantum cost of 18 and delay of 18 Δ.

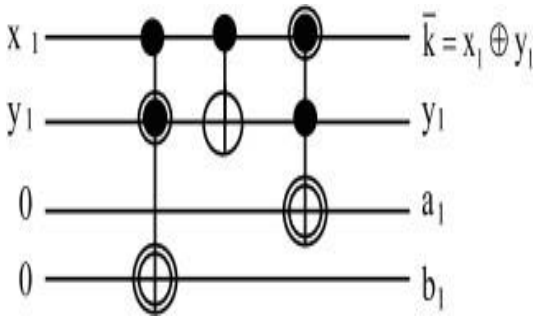

Fig. 1Reversible implementation of R-B comp

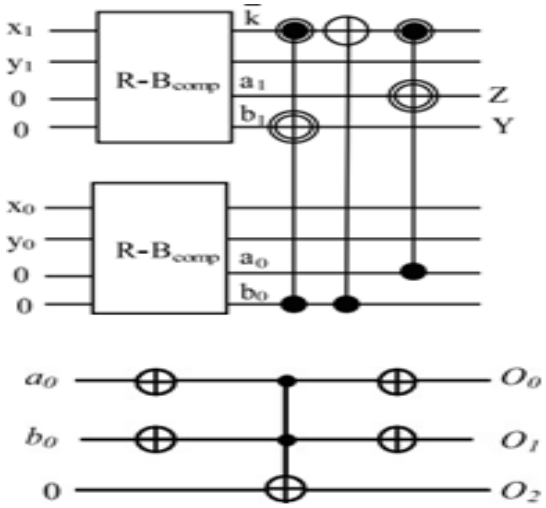

Fig.2 Reversible implementation of 2 bit comparator and output circuit

PROPOSED COMPARATOR DESIGN

2 Bit improved Comparator design

The proposed 2 bit comparator is constructed using TR and UPG gates. In this design 2 bit comparator requires less number of constant inputs, less quantum cost and delay. Hence it aids for the improvement of overall performance of the comparator tree.

Here TR gate 1 generates B1=x1⊕y1, A1=y1x1' and TR gate 2 generates B0=x0⊕y0, A0=y0x0'. Using feymann gate with B0 and 0 as inputs, B0 is generated twice which is given to TR gate 3 and UPG gates. TR gate 3 generates S= x1'y1(x0⊕y0)' ⊕x0y0' which is less than equation. UPG gate gives us equal to equation i.e. T=(x0⊕y0)' (x1⊕y1)'. To get x>y equation we need to extract (S+T)' equation. It can be modified as (S⊕T)' as S=1 and T=1 case doesn't exist. On giving S and T as inputs to feymann gate we gate S⊕T and S, where S is one of our required outputs which gives x<y. S⊕T on passing through NOT gate produces (S⊕T)' which gives x>y. Hence, both outputs are extracted using the proposed 2 bit design with Quantum cost 18 and delay 11Δ.

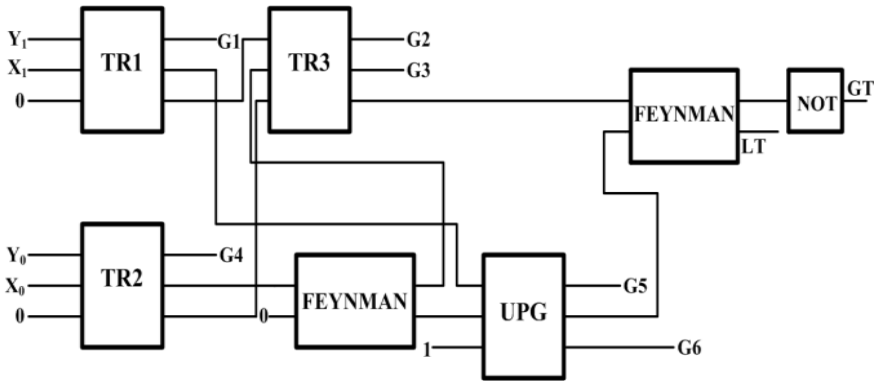

Fig.3 Block diagram of reversible 2 bit comparator circuit

The quantum cost and delay can be further reduced by using the below output circuit as it has Quantum cost and delay as 2 and 2Δ.

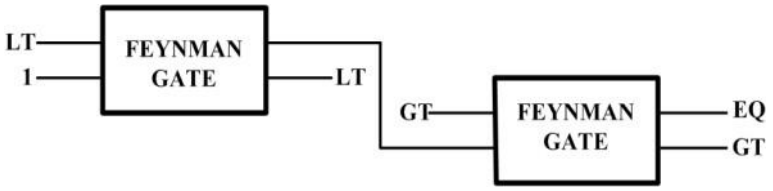

Fig.4 Block diagram of reversible output circuitary

8-bit reversible comparator

The proposed design of the 8-bit reversible comparator using reversible 2-bit comparator is shown in Fig.6 (the garbage outputs in the design are not shown). The design contains 2-bit reversible binary comparators as the nodes of the binary tree. Since n=8, the tree will have log2(8)= 3 levels. The design requires seven 2-bit binary comparators along with a reversible output circuitry.

The quantum cost of reversible 8 bit comparator is 7*(quantum cost of 2 bit reversible comparator) + quantum cost of output circuit that is 7*(17)+2=121. Similarly delay of reversible 8 bit comparator is 3*(delay of 2-bit reversible comparator) +delay of output circuit that is 3*(10)+2=32.

	QC (Quantum Cost)	Delay	GO(Garbage Outputs)
Serial design	321	199	64
Existing design[1]	135	61	42
Proposed Design	128	35	42

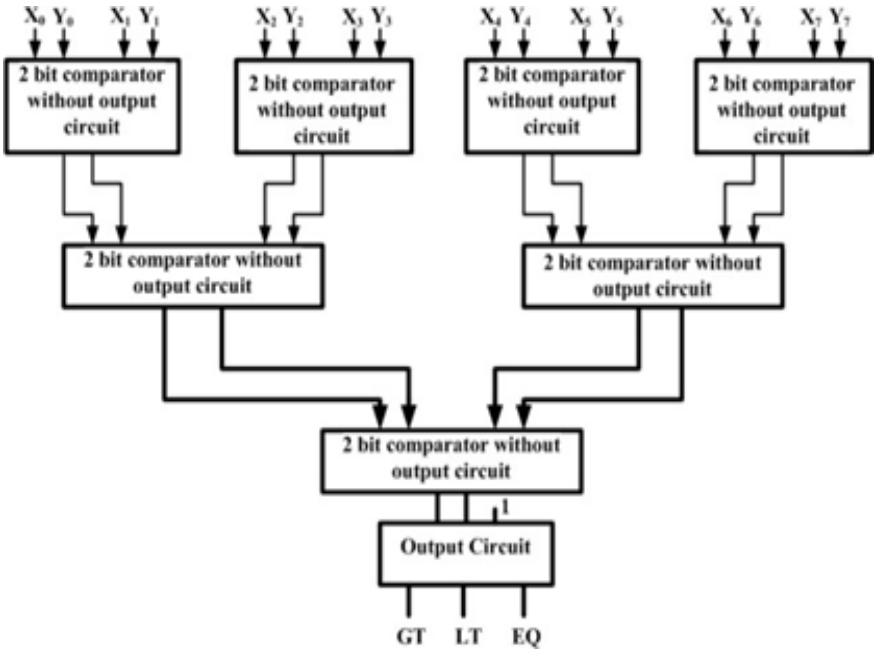

Fig. 5 Block diagram of Reversible 8-Bit reversible comparator

64 bit reversible comparator

The proposed design of the 64-bit reversible comparator using reversible 8-bit comparator is shown in Fig. (the garbage outputs in the design are not shown). The design contains 8-bit reversible binary comparators as the nodes of the binary tree. Since n=64, the tree will have log8(64)= 2 levels. The design requires nine 8-bit binary comparators along with a reversible output circuitry. The quantum cost of reversible 64 bit comparator is 9*(quantum cost of 8 bit reversible comparator without output circuit)+ quantum cost of output circuit that is 9*(119)+2=1073. Similarly delay of reversible 64 bit comparator is 2*(delay of 8 bit reversible comparator without output circuit)+ delay of output circuit that is 2*(30)+2=62.

	QC (Quantum Cost)	Delay	GO(Garbage Outputs)
Serial design	2505	1543	512
Existing design[1]	1143	115	378
Proposed Design	1136	68	378

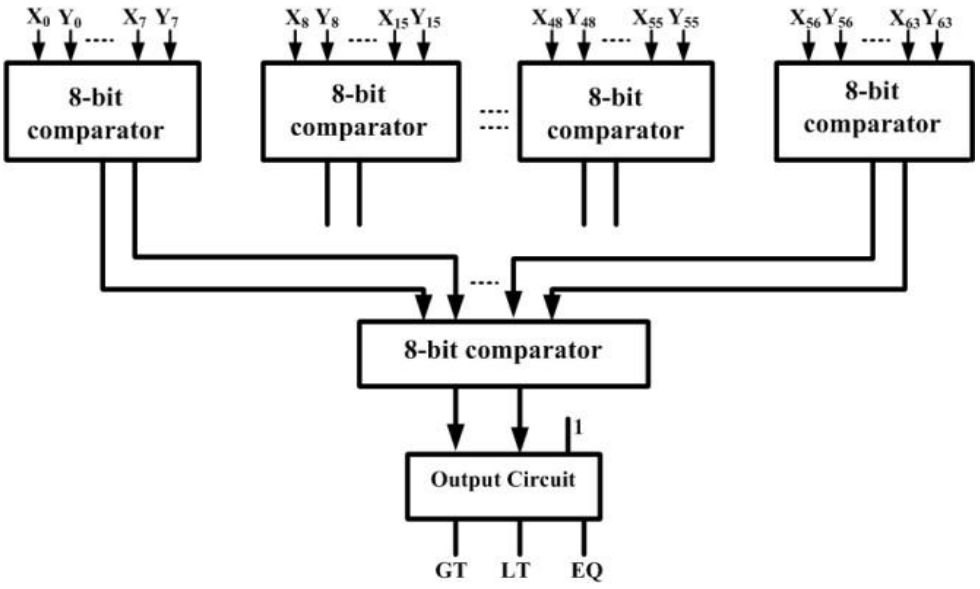

Fig.6 Block diagram of Reversible 64-Bit reversible comparator

SIMULATION RESULTS

Fig. a Simulation of Reversible 8-Bit reversible comparator

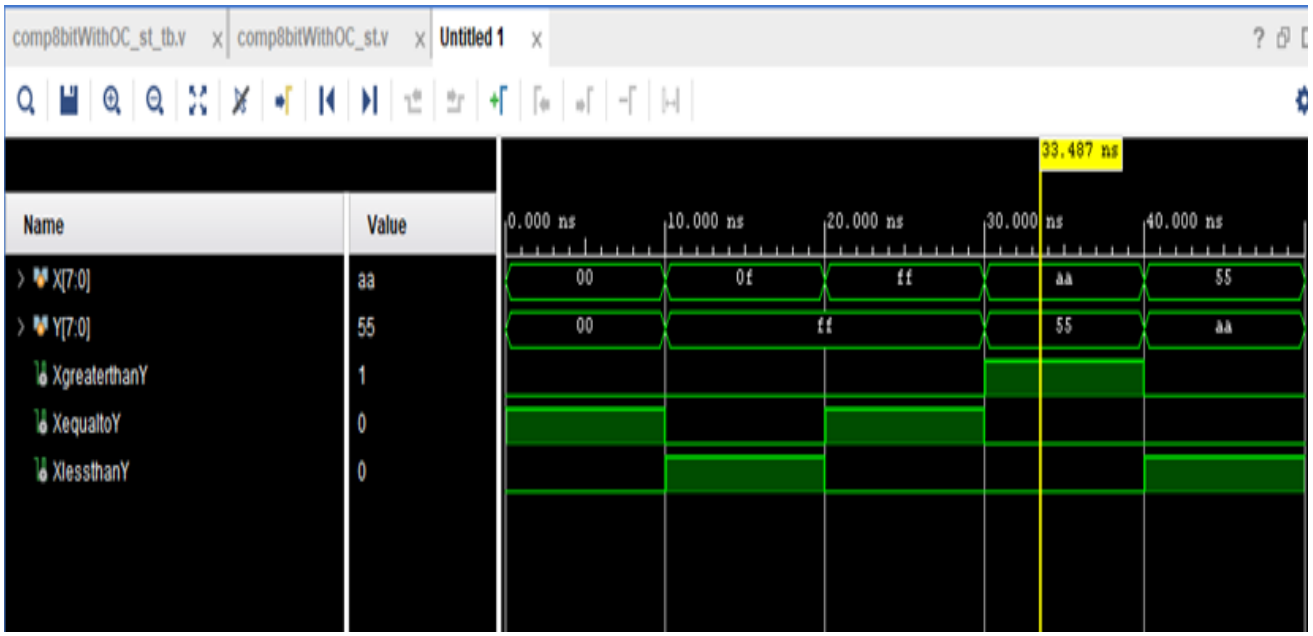

Fig. b Simulation of Reversible 64-Bit reversible comparator

CONCLUSION

The development of high-speed, low-delay comparators is crucial for modern digital systems, and the proposed 2-bit comparator design using TR and UPG gates significantly enhances performance by reducing

quantum cost and delay. This innovative approach allows for scalable construction of larger comparators, enabling the efficient design of 4, 8, 16, 32, and 64-bit comparators, which can be easily adapted for n-bit comparator trees by setting the MSB bits to zero. This scalability and flexibility ensure improved overall circuit performance, making the design a versatile and efficient solution for various digital applications. The proposed design not only meets the current demands for high-speed comparators but also sets a foundation for future advancements in reversible computing, leading to more energy-efficient digital systems.

FUTURE WORK

The future scope of the novel design of comparator trees based on reversible logic is vast and promising. One significant area of focus is optimizing the design for larger bit comparators, such as those exceeding 64 bits, which will require advanced techniques to manage increased complexity and resource demands efficiently. Integrating these comparators into quantum algorithms, like quantum sorting and search algorithms, can further enhance the performance of these computational tasks. Additionally, ongoing research aimed at minimizing quantum cost and delay, through new configurations and gate optimizations, will be crucial for improving efficiency. Addressing error correction and fault tolerance is another critical aspect, ensuring reliable operation under noisy conditions, essential for practical quantum computing applications.

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